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PATENT
(5500-78100/TT4934)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 09/927,054
Filed: August 9, 2001
Inventor(s):
Kevin J. McGrath

§ Examiner: Unknown
§ Group/Art Unit: 2183
§ Atty. Dkt. No: 5500-78100
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Title: Instruction Causing Swap of
Segment Register and
Another Register

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Lawrence J. Merkel

Name of Registered Representative

Signature

November 15, 2001

Date

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Group 2100

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☒ the additional information identified below in paragraph 3. A copy of each reference listed on the Form PTO-1449 is enclosed.

1. This Information Disclosure Statement is submitted:

- a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
☒ before the mailing date of a first Office Action on the merits; or
☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.
- b. ☐ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☐ a fee of \$180.00 is enclosed.
- c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of \$180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☒ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

pp. 1-3, entitled "Background of the Invention," from the captioned application specification.

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Conley, Rose & Tayon, P.C. Deposit Account No. 50-1505/5500-78100/LJM.

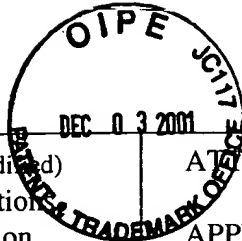
Respectfully submitted,



Lawrence J. Merkel
Reg. No. 41,191
Agent for Applicant(s)

CONLEY, ROSE & TAYON, P.C.
P. O. Box 398
Austin, Texas 78767
(512) 476-1400

Date: November 15, 2001



Form PTO-1449 (modified)
List of Patents and Publications
For Applicant's Information
Disclosure Statement
(Use several sheets if necessary)

ATTY. DKT. NO. 5500-78100

SERIAL NO. 09/927,054

APPLICANT: McGrath

GROUP: 2183

FILING DATE: August 9, 2001

U.S. PATENT DOCUMENTS

	A9	5,684,993	11/4/97	Willman		
	A18	5,418,956	5/23/95	Willman		

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	A1	<u>The Technology Behind Crusoe™ Processors, Low-Power x86-Compatible Processors Implemented with Code Morphing™ Software</u> , Transmeta Corporation, January 2000, pages 1-18.
	A2	<u>Alpha Learns to Do Windows; Digital's FX!32 is The Key To Running Win32 Software on Alpha/Windows NT.</u> , Selinda Chiquoine, BYTE, August 4, 1998, 4 pages.
	A3	<u>Awards Stack Up for DIGITAL FX!32 Windows Compatibility Software for ALPHA</u> , DIGITAL Press Releases, December 11, 1997, 7 pages.
	A4	<u>DIGITAL FX!32; White Paper: How DIGITAL FX!32 Works</u> , DIGITAL Semiconductor, January 26, 1998, 4 pages.
	A5	<u>An Alpha in PC Clothing; Digital Equipment's New x86 Emulator Technology Makes An Alpha System a Fast x86 Clone</u> , Tom Thompson, BYTE, August 4, 1998, 7 pages.
	A6	<u>AMD 64-Bit Technology; The AMD x86 Architecture Programmers Overview</u> , AMD, Publication #24108 Rev: A, August 2000, pages 1-106.
	A7	<u>AMD 64-Bit Technology; The AMD x86-64 Architecture Programmers Overview</u> , AMD, Publication #24108 Rev: C, January 2001, pages 1-128.
	A8	<u>Alpha Architecture Reference Manual</u> , Third Edition, Digital Press, 1998 Digital Equipment Corporation, pages 5-14 to 5-15, 5-18 to 5-19, 5-30 to 5-35.
	A10	<u>32-Bit Microprocessor User's Manual</u> , MC68020, Third Edition, Motorola, 1989, pp. 3-105 and 3-184..
	A11	<u>Intel Architecture Software Developer's Manual</u> , Volume 1: Basic Architecture, 1997, pages 6-17 to 6-19.
	A12	Intel, "Intel Architecture Software Developer's Manual, Vol. 2: Instruction Set Reference," 1997, pages 3-29, 3-66 to 3-69, 3-196 to 3-197, 3-460 to 3-463..
	A13	AMD, "SYSCALL and SYSRET Instruction Specification", Application Note, 1998, pages 1-10.
	A14	Intel, "Intel Architecture Software Developer's Manual, Vol. 2: Instruction Set Reference," 1997, pages 3-256 to 3-258, 3-286 to 3-290, 3-350 to 3-353, 3-385 to 3-387.
	A15	<u>Intel Architecture Software Developer's Manual</u> , Volume 1: Basic Architecture, 1997, pages 3-38 to 3-39.
	A16	<u>Addendum-Intel Architecture Software Developer's Manual</u> , Vol. 2: Instruction Set Reference, 1996/1997, Chapter 3, pages 3-1 to 3-15.
	A17	<u>Pentium Pro Family Developer's Manual</u> , Volume 3: Operating System Writer's Guide, 1996, pages 2-1 to 2-21, 3-1 to 3-33, 4-1 to 4-29.

EXAMINER:

DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Information Disclosure Statement--PTO 1449 (modified)